

multiple transition detection circuits, each coupled to one of the sampling chains such that, for each time a logic level of a delayed version of the derived clock signal is different at successive sampling times of the known clock signal, a transition detection circuit produces as an output signal thereof a transition indication value; and

a combining circuit for logically combining output signals of the transition detection circuits.

6. The apparatus of claim 5, wherein the combining circuit comprises a summation element for forming a sum of transition values and decision logic for comparing the sum to a threshold value.
7. The apparatus of claim 6, wherein the threshold value is set in accordance with an anticipated frequency range of the unknown clock signal.
8. A method of forming a number stream representing frequency or phase of digital or digitized clock signals using a digital circuit, one of the clock signals being a known clock signal and another of the clock signal being an unknown clock signal, comprising:
 - applying to the digital circuit an alias value indicating an expected frequency range of the unknown clock signal; and
 - forming the number stream in accordance with the alias value.
9. A digital circuit for forming a number stream for representing frequency or phase of digital or digitized clock signals, one of the clock signals being a known clock signal and another of the clock signal being an unknown clock signal, comprising:
 - a first logic section including multiple chains of flip flops, each chain producing an intermediate values; and
 - a second logic section for receiving an alias value indicating an expected frequency range of the unknown clock signal and combining the intermediate values to form the number stream.